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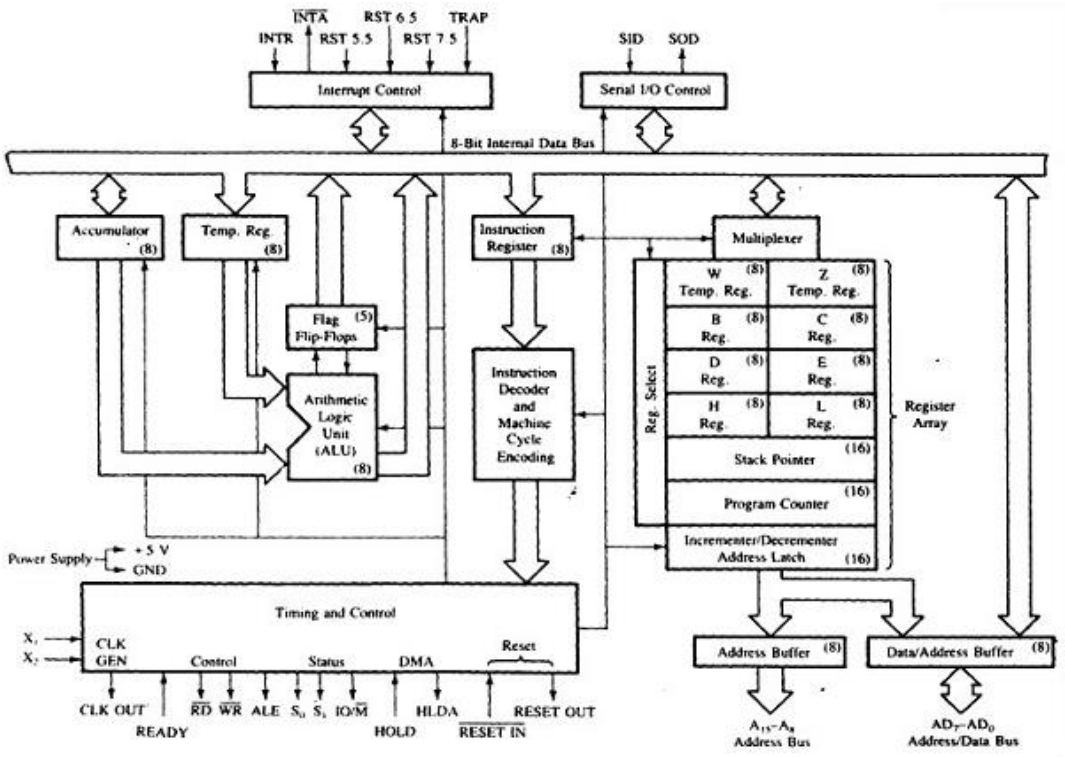
UNIT V

Q1. Draw and explain the architecture of 8085 microprocessor

Ans: 8085 Architecture is shown in figure



Architecture of 8085 Microprocessor

8085 consists of various units and each unit performs its own functions. The various units of a microprocessor are listed below

· Accumulator

· Arithmetic and logic Unit

· General purpose register

· Program counter

· Stack pointer

· Temporary register

· Flags

· Instruction register and Decoder

· Timing and Control unit

· Interrupt control

· Serial Input/output control

· Address buffer and Address-Data buffer

· Address bus and Data bus

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8085 Microprocessor – Functional Units

Accumulator

It is an 8-bit register used to perform arithmetic, logical, I/O & LOAD/STORE operations. It is connected to internal data bus & ALU.

Arithmetic and logic unit

As the name suggests, it performs arithmetic and logical operations like Addition, Subtraction, AND, OR, etc. on 8-bit data.

General purpose register

There are 6 general purpose registers in 8085 processor, i.e. B, C, D, E, H & L. Each register can hold 8-bit data.

These registers can work in pair to hold 16-bit data and their pairing combination is like B-C, D-E & H-L.

Program counter

It is a 16-bit register used to store the memory address location of the next instruction to be executed. Microprocessor increments the program whenever an instruction is being executed, so that the program counter points to the memory address of the next instruction that is going to be executed.

Stack pointer

It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.

Temporary register

It is an 8-bit register, which holds the temporary data of arithmetic and logical operations.

Flag register

It is an 8-bit register having five 1-bit flip-flops, which holds either 0 or 1 depending upon the result stored in the accumulator.

These are the set of 5 flip-flops −

- Sign (S)
- Zero (Z)
- Auxiliary Carry (AC)
- Parity (P)
- Carry (C)

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Its bit position is shown in the following table −

D7	D6	D5	D4	D3	D2	D1	D0
S	Z		AC		P		CY

Instruction register and decoder
It is an 8-bit register. When an instruction is fetched from memory then it is stored in the Instruction register. Instruction decoder decodes the information present in the Instruction register.

Timing and control unit
It provides timing and control signal to the microprocessor to perform operations. Following are the timing and control signals, which control external and internal circuits −

- Control Signals: READY, RD', WR', ALE
- Status Signals: S0, S1, IO/M'
- DMA Signals: HOLD, HLDA
- RESET Signals: RESET IN, RESET OUT

Interrupt control
As the name suggests it controls the interrupts during a process. When a microprocessor is executing a main program and whenever an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request. After the request is completed, the control goes back to the main program.
There are 5 interrupt signals in 8085 microprocessor: INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

Serial Input/output control
It controls the serial data communication by using these two instructions: SID (Serial input data) and SOD (Serial output data).

Address buffer and address-data buffer
The content stored in the stack pointer and program counter is loaded into the address buffer and address-data buffer to communicate with the CPU. The memory and I/O chips are connected to these buses; the CPU can exchange the desired data with the memory and I/O chips.

Address bus and data bus
Data bus carries the data to be stored. It is bidirectional, whereas address bus carries the location to where it should be stored and it is unidirectional. It is used to transfer the data & Address I/O devices.

Q2. Give the format of Flag register in 8085. Explain each flag.
Ans: The **Flag register** is a Special Purpose Register. Depending upon the value of result after any arithmetic and logical operation the flag bits become set (1) or reset (0). In 8085 microprocessor, flag register consists of 8 bits and only 5 of them are useful. It is an 8-bit register having five 1-bit flip-flops, which holds either 0 or 1 depending upon the result stored in the accumulator.
The 5 flags are:

These are the set of 5 flip-flops −

- Sign (S)
- Zero (Z)
- Auxiliary Carry (AC)
- Parity (P)
- Carry (C)

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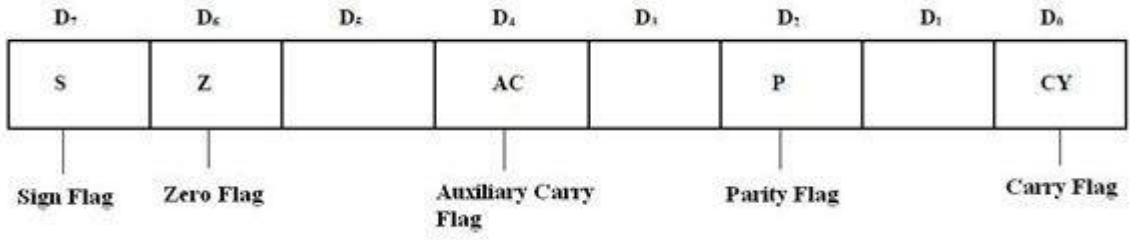
Its bit position is shown in the following table −



1) **The carry flag(CF):-**
This flag is set whenever there has been a carry out of, or a borrow into, the higher order bit of the result. The flag is used by the instructions that add and subtract multi byte numbers.
1-carry out from MSB bit on addition or borrow into MSB bit on subtraction
0-no carry out or borrow into MSB bit
2) **The parity flag(PF):-**
This flag is set whenever the result has even parity, an even number of 1 bits. If parity is odd, PF is cleared.
1-low byte has even number of 1 bits
0-low byte has odd parity
3) **The auxiliary carry flag(AF):-**
This flag is set whenever there has been a carry out of the lower nibble into the higher nibble or a borrow from higher nibble into the lower nibble of an 8 bit quantity, else AF is reset. This flag is used by decimal arithmetic instructions.
1-carry out from bit 3 on addition or borrow into bit 3 on subtraction
0-otherwise
4) **The zero flag(ZF):-**
This flag is set, when the result of operation is zero, else it is reset.
1-zero result
0-non-zero result
5) **The sign flag(SF):-**
This flag is set, when MSB (Most Significant Bit) of the result is 1. Since negative binary numbers are represented in the 8085 CPU in standard two's complement notation, SF indicates sign of the result.
1-MSB is 1 (negative)
0-MSB is 0 (positive)

3. Explain all addressing modes of µp 8085.
Ans: **Addressing Modes in 8085**
These are the instructions used to transfer the data from one register to another register, from the memory to the register, and from the register to the memory without any alteration in the content.
Addressing modes in 8085 is classified into 5 groups −
Immediate addressing mode
In this mode, the 8/16-bit data is specified in the instruction itself as one of its operand.
For example: MVI K, 20F: means 20F is copied into register K.
Register addressing mode
In this mode, the data is copied from one register to another.
For example:MOV K, B: means data in register B is copied to register K.
Direct addressing mode

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In this mode, the data is directly copied from the given address to the register.
For example: LDB 5000K: means the data at address 5000K is copied to register B.

Indirect addressing mode

In this mode, the data is transferred from one register to another by using the address pointed by the register.
For example: MOV K, B: means data is transferred from the memory address pointed by the register to the register K.

Implied addressing mode

This mode doesn't require any operand; the data is specified by the opcode itself.
For example: CMP.

UNIT VI

4. Explain interrupt structure of microprocessor 8085 in detail.

Ans:

- Interrupt is signals send by an external device to the processor, to request the processor to perform a particular task or work.
- Mainly in the microprocessor based system the interrupts are used for data transfer between the peripheral and the microprocessor.
- The processor will check the interrupts always at the 2nd T-state of last machine cycle.
- If there is any interrupt it accept the interrupt and send the INTA (active low) signal to the peripheral.
- The vectored address of particular interrupt is stored in program counter.
- The processor executes an interrupt service routine (ISR) addressed in program counter.
- It returned to main program by RET instruction.

Types of Interrupts:

It supports two types of interrupts.

- **Hardware**
- **Software**

Software interrupts:

- The software interrupts are program instructions. These instructions are inserted at desired locations in a program.
- The 8085 has eight software interrupts from RST 0 to RST 7. The vector address for these interrupts can be calculated as follows.
- Interrupt number * 8 = vector address
- For RST 5,5 * 8 = 40 = 28H
- Vector address for interrupt RST 5 is 0028H

The Table shows the vector addresses of all interrupts.

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Interrupt	Vector address
RST 0 RST 1	0000_H 0008_H
RST 2 RST 3	0010_H 0018_H
RST 4 RST 5	0020_H 0028_H
RST 6 RST 7	0030_H 0038_H

Hardware interrupts:

- An external device initiates the hardware interrupts and placing an appropriate signal at the interrupt pin of the processor.
- If the interrupt is accepted then the processor executes an interrupt service routine.

The 8085 has five hardware interrupts

(1) TRAP (2) RST 7.5 (3) RST 6.5 (4) RST 5.5 (5) INTR

Interrupt	Vector address
RST 7.5	$003C_H$
RST 6.5	0034_H
RST 5.5	$002C_H$
TRAP	0024_H

TRAP:

- This interrupt is a non-maskable interrupt. It is unaffected by any mask or interrupt enable.
- TRAP bas the highest priority and vectored interrupt.
- TRAP interrupt is edge and level triggered. This means hat the TRAP must go high and remain high until it is acknowledged.
- In sudden power failure, it executes a ISR and send the data from main memory to backup memory.
- The signal, which overrides the TRAP, is HOLD signal. (i.e., If the processor receives HOLD and TRAP at the same time then HOLD is recognized first and then TRAP is recognized).

RST 7.5:

The RST 7.5 interrupt is a maskable interrupt.

- It has the second highest priority.
- It is edge sensitive. ie. Input goes to high and no need to maintain high state until it recognized.
- Maskable interrupt. It is disabled by,

1.DI instruction
2.System or processor reset.
3.After reorganization of interrupt.

- Enabled by EI instruction.

RST 6.5 and 5.5:

- The RST 6.5 and RST 5.5 both are level triggered. . ie. Input goes to high and stay high until it recognized.
- Maskable interrupt. It is disabled by,

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1.DI, SIM instruction
2.System or processor reset.
3.After reorganization of interrupt.

- Enabled by EI instruction.
- The RST 6.5 has the third priority whereas RST 5.5 has the fourth priority.

INTR:

- INTR is a maskable interrupt. It is disabled by,

1.DI, SIM instruction
2.System or processor reset.
3.After reorganization of interrupt.

- Enabled by EI instruction.
- Non- vectored interrupt. After receiving INTA (active low) signal, it has to supply the address of ISR.
- It has lowest priority.
- It is a level sensitive interrupts. i.e. Input goes to high and it is necessary to maintain high state until it recognized.

5. Differentiate between maskable & Nonmaskable interrupts.

Ans:

Maskable Interrupts: are those which can be disabled or ignored by the microprocessor. These interrupts are either edge-triggered or level-triggered, so they can be disabled. *INTR, RST 7.5, RST 6.5, RST 5.5* are maskable interrupts in 8085 microprocessor.

Non-Maskable Interrupts: are those which cannot be disabled or ignored by microprocessor. *TRAP* is a non-maskable interrupt. It consists of both level as well as edge triggering and is used in critical power failure conditions.

6. Write a program to find larger number out of two given number.

Ans:

2000	LDA 2050	A<-25
2003	MOV B, A	B<-25
2004	LDA 2051	A<-15
2007	CMP B	A-B
2008	JNC 200C	Jump if Carry flag is Reset(Carry flag = 0)
200B	MOV A, B	A<-25
200C	STA 3050	3050<-25

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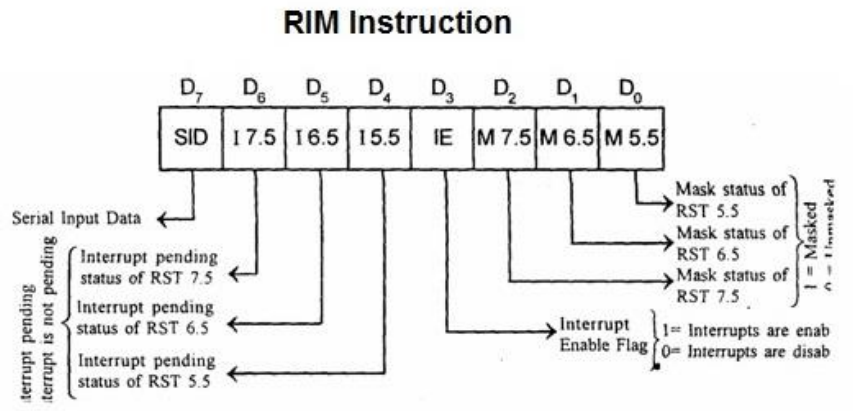
7. Explain the following instructions of µp 8085.
(1) RIM
(2) SIM
(3) EI
(4) DI.
Ans
(1) RIM : **RIM** is Read Interrupt Mask. Used to check whether the interrupt is Masked or not. When RIM instruction is executed an 8-bit data is loaded in accumulator, which can be interpreted as shown in fig.



Bit D7 (SID-Serial Input Data) This is the input pin of the serial data interface which is connected to pin 5 of the 8085, and indicates the high/low status of that pin.
Bits D6-D4 (I 7.5, I 6.5, I 5.5) These bits indicates that an interrupt is pending for these three 8085 interrupts 7.5, 6.5, and 5.5. If interrupts 5.5 or 6.5 have been masked off by bits D0 or D1, bits D4 and D5 will not be set. Bit D6, which corresponds to the 7.5 interrupt, will be set on to indicate that an interrupt 7.5 was requested, even if it was masked off.
Bit D3 (IE-Interrupt Enable) This bit indicates whether interrupts are enabled (1) using the EI (Enable Interrupts) instruction, or disabled (0) using the DI (Disable Interrupts) instruction.
Bits 2-D0 (M 7.5, M6.5, M5.5) Mask status of interrupts 7.5, 6.5, and 5.5. Corresponds to bits D2-D0 of the SIM instruction. 1 if masked, 0 if enabled.

(2) SIM : The SIM instruction uses the data in the accumulator as follows:

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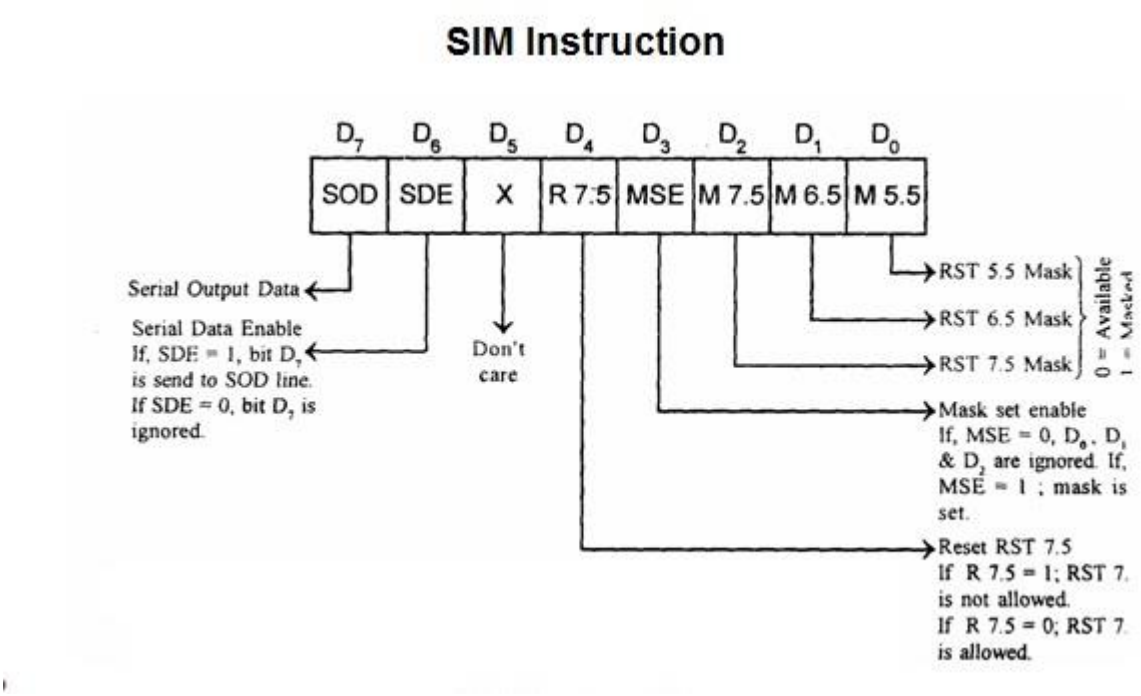

D7-D6 - The left two bits are related to the serial interface. When D6 (SDE-Serial Data Enable) is 1, then whatever is in D7 (SOD-Serial Data Output) is written to the serial data output (pin 4 of the 8085). If D6=0, nothing is written. This allows a SIM instruction to be executed altering interrupt masks without affecting serial data.
Bit D5 is not used.
Bit D4 (R 7.5-Reset RST 7.5) This bit allows the SIM instruction to reset the interrupt pending flag indicated by bit D6 in the RIM instruction layout. The 7.5 interrupt can indicate that it is pending via the RIM instruction even though it is masked off. This bit allows that pending request to be reset.
Bit D3 (MSE-Mask Set Enable) is like SDE -- it indicates whether the lower three bits (D2-D0) are ignored or not. This allows the serial data output to occur without affecting the interrupt masks. If a SIM is executed with this bit low, the condition of the mask bits will not change. If a SIM is executed with this bit set high, the mask bits will be set according to the lower three bits of the accumulator.
Bits D2-D0 (RST 7.5 Mask, RST .5 Mask, RST 5.5 Mask) These are the interrupt masks for the 8085 interrupts 7.5, 6.5, and 5.5. If the corresponding bit is 0, the interrupt is enabled. If the bit is 1, the interrupt is masked (ignored)

(3)EI: The interrupt enable flip-flop is set and all interrupts are enabled. No flags are affected. After a system reset or the acknowledgement of an interrupt, the interrupt enable flipflop is reset, thus disabling the interrupts. This instruction is necessary to reenable the interrupts (except TRAP).

Eg: - EI

(4)DI: The interrupt enable flip-flop is reset and all the interrupts except the TRAP are disabled. No flags are affected.

Eg: - DI

8. Draw and explain Memory Read Machine cycle in detail.

Ans: The memory read timing diagram can be explained as below:

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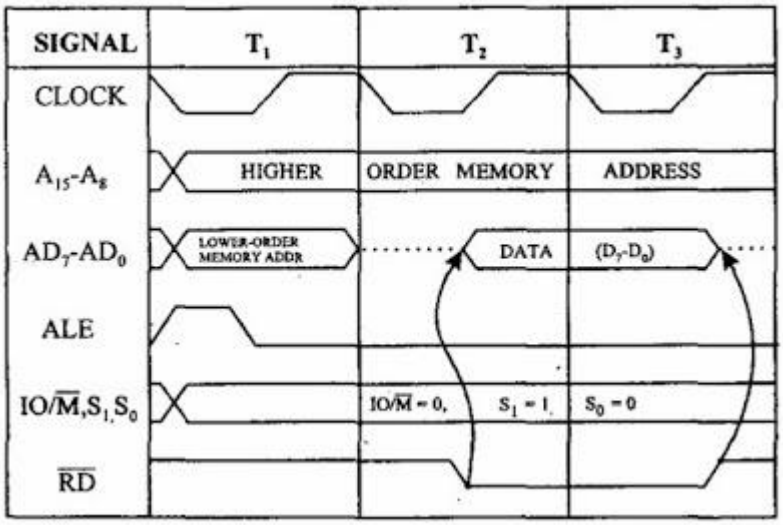
- The MP places the 16-bit memory address from the program counter on address bus. At time period T1, the higher order memory address is placed on the address lines A15 – A8. When ALE is high, the lower address is placed on the bus AD7 – AD0. The status signal IO/M(bar) goes low indicating the memory operation and two status signals S1 = 1, S0 = 0 to indicate memory read operation.
- At time period T2, the MP sends RD(bar) control line to enable the memory read. When memory is enabled with RD(bar) signal, the data from the addressed memory location is placed on the data bus with ALE low.
- The data is reached at processor register during T3 state. When data is arrived, the RD(bar) signal goes high. It causes the bus to go into high impedance state.



9. Explain EI and DI instruction of µp 8085.

Ans: EI: The interrupt enable flip-flop is set and all interrupts are enabled. No flags are affected. After a system reset or the acknowledgement of an interrupt, the interrupt enable flipflop is reset, thus disabling the interrupts. This instruction is necessary to reenable the interrupts (except TRAP).

Eg: - EI

DI: The interrupt enable flip-flop is reset and all the interrupts except the TRAP are disabled. No flags are affected.

Eg: - DI

10. Explain Hardware Interrupt structure of µp 8085.

Ans: Hardware Interrrupts given below:
TRAP
RST7.5
RST6.5
RST5.5

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INTR
INTA is not an interrupt. INTA is used by the Microprocessor for sending the acknowledgement. TRAP has highest priority and RST7.5 has second highest priority and so on. The Vector address of these interrupts are given below:

Interrupt	Vector address
RST 7.5	$003C_H$
RST 6.5	0034_H
RST 5.5	$002C_H$
TRAP	0024_H

1.TRAP:-It is non maskable edge and level triggered interrupt. TRAP has the highest priority and vectores interrupt. Edge and level triggeredmeans that the TRAP must go high and remain high until it is acknowledged. In case of sudden power failure, it executes a ISR and send the data from main memory to backup memory.
As we know that TRAP can not be masked but it can be delayed using HOLD signal.
This interrupt transfers the microprocessor's control to location 0024H.
How a TRAP interrupt may be masked???
TRAP interrupts can only be masked by reseting the microprocessor. There is no other way to mask it.

2.RST7.5:-It has the second highest priority. It is maskable and edge level triggered interrupt. The vector address of this interrupt is 003CH. Edge sensitive means input goes high and no need to maintain high state until it is recognized.
How It may be masked??
It can also be reset or masked by reseting microprocessor. It can also be resetted by DI instruction.

3.RST6.5 and RST5.5:-These are level triggered and maskable interrupts. When RST6.5 pin is at logic 1, INTE flip-flop is set. RST 6.5 has third highest priority and RST 5.5 has fourth highest priority.
It can be masked by giving DI and SIM instructions or by reseting microprocessor.

4.INTR:-It is level triggered and maskable interrupt. It has the lowest priority. It can be disabled by resetting the microprocessor or by DI and SIM instruction.

The following sequence of events occurs when INTR signal goes high:
1. The 8085 checks the status of INTR signal during execution of each instruction.

2. If INTR signal is high, then 8085 complete its current instruction and sends active low interrupt acknowledge signal, if the interrupt is enabled.

3.On receiving the instruction, the 8085 save the address of next instruction on stack and execute received instruction.

11. Write a program to shift 10 bytes of data from memory location 8000 H to 9000 H.
Ans

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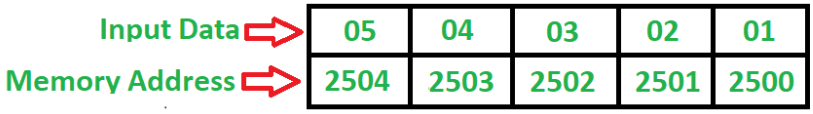

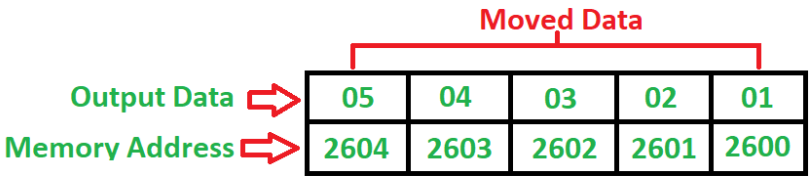

Algorithm –

1. Load register pair H-L with the address 2500H
2. Load register pair D-E with the address 2600H
3. Move the content at memory location into accumulator
4. Store the content of accumulator into memory pointed by D-E
5. Increment value of register pair H-L and D-E by 1
6. Decrements value of register C by 1
7. If zero flag not equal to 1, go to step 3
8. Stop

Program –

MEMORY	MNEMONICS	OPERANDS	COMMENT
2000	MVI	C, 05	[C] <- 05
2002	LXI	H, 2500	[H-L] <- 2500
2005	LXI	D, 2600	[D-E] <- 2600
2008	MOV	A, M	[A] <- [[H-L]]
2009	STAX	D	[A] -> [[D-E]]
200A	INX	H	[H-L] <- [H-L] + 1
200B	INX	D	[D-E] <- [D-E] + 1
200C	DCR	C	[C] <- [C] – 1
200D	JNZ	2008	Jump if not zero to 2008
2010	HLT		Stop

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12. Write a program to add two 16 bit data present in memory from location 4000 H and place the result starting at 4001 H.

Ans

Add the 16-bit number in memory locations 4000H and 4001H to the 16-bit number in memory locations 4002H and 4003H. The most significant eight bits of the two numbers to be added are in memory locations 4001H and 4003H. Store the result in memory locations 4004H and 4005H with the most significant byte in memory location 4005H.

1. Sample problem:
2. (4000H) = 15H
3. (4001H) = 1CH
4. (4002H) = B7H
5. (4003H) = 5AH
6. Result = 1C15 + 5AB7H = 76CCH
7. (4004H) = CCH
8. (4005H) = 76H

Source Program 1:

9. LHLD 4000H : "Get first I6-bit number in HL"
10. XCHG : "Save first I6-bit number in DE"
11. LHLD 4002H : "Get second I6-bit number in HL"
12. MOV A, E : "Get lower byte of the first number"
13. ADD L : "Add lower byte of the second number"
14. MOV L, A : "Store result in L register"
15. MOV A, D : "Get higher byte of the first number"
16. ADC H : "Add higher byte of the second number with CARRY"
17. MOV H, A : "Store result in H register"
18. SHLD 4004H : "Store I6-bit result in memory locations 4004H and 4005H"
19. HLT : "Terminate program execution"

13. Write an ALP to find the number of one's in a given 8 – bit data present of 4100 H.

Ans

Algorithm –

1. Move 00 to register B immediately for count
2. Move 08 to register C immediately for shifting
3. Load the data of memory [3000] into accumulator
4. Rotate ‘A’ right with carry
5. Jump if no carry to step-7
6. Otherwise increase register B by 1
7. Decrease register C by 1
8. Jump if not zero to step-4
9. Move content of register B into accumulator
10. Store content of accumulator into memory [3001] (**number of count**)
11. Stop

Program –

MEMORY	MNEMONICS	OPERANDS	COMMENT
2000	MVI	B, 00	[B] <- 00
2002	MVI	C, 08	[C] <- 08
2004	LDA	[3000]	[A] <- [3000]

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MEMORY	MNEMONICS	OPERANDS	COMMENT
2007	RAR		rotate 'A' right with carry
2008	JNC	200C	jump if no carry
200B	INR	B	[B] <- [B] + 1
200C	DCR	C	[C] <- [C] – 1
200D	JNZ	2007	jump if not zero
2010	MOV	A, B	[A] <- [B]
2011	STA	[3001]	number of once
2014	HLT		Stop

14. Write a program to find the greatest number in the block of 10 bytes which are present in memory location from address 7000H. Store the greatest number at location 8000H.

Ans

Store the maximum number in memory location 2300H. Assume that the numbers in the block are all 8 bit unsigned binary numbers

Sample problem
(2200H) = 04
(2201H) = 34H
(2202H) = A9H
(2203H) = 78H
(2204H) =56H
Result = (2202H) = A9H
Source program
LDA 2200H
MOV C, A : Initialize counter
XRA A : Maximum = Minimum possible value = 0
LXI H, 2201H : Initialize pointer
BACK: CMP M : Is number> maximum
JNC SKIP : Yes, replace maximum
MOV A, M
SKIP: INX H
DCR C
JNZ BACK
STA 2300H : Store maximum number
HLT : Terminate program execution